WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array comprising a plurality of memory cells and cell select circuitry configured to selectively connect the plurality of memory cells to a data line;

a bias circuit operative to charge the data line to a bias voltage responsive to a bias enable signal; and

a sense amplifier circuit having an input coupled to the data line and including an output buffer, the sense amplifier circuit operative to drive the output buffer according to a voltage on the data line responsive to a sense enable signal to thereby generate a sense amplifier output signal indicative of a state of a memory cell connected to the data line.

2. A device according to Claim 1, wherein the bias circuit comprises:

a buffer having an input coupled to the data line and operative to be enabled and disabled responsive to the bias enable signal;

a first transistor having a drain coupled to the input of the buffer, a source coupled to a power supply node and a gate coupled to an output of the buffer; and

a second transistor having a source coupled to the power supply node, a drain coupled to the output of the buffer, and a gate coupled to the bias enable signal.

3. A device according to Claim 2, wherein the first and second transistors comprise respective PMOS transistors.

4. A device according to Claim 1, wherein the sense amplifier circuit comprises:

first and second complementary transistors coupled in series between the data line and the power supply node and coupled to an input of the output buffer at a junction of the first and second transistors; and

a sense enable circuit coupled to the data line and to a gate of the first transistor, the sense enable circuit operative to drive the gate of the first transistor responsive to the sense amplifier enable signal.

5. A device according to Claim 4, wherein the sense enable circuit comprises:

an inverter having an input coupled to the data line and an output coupled to the gate of the first transistor, the inverter operative to be enabled and disabled responsive to the sense amplifier; and

a third transistor having a drain coupled to an output of the inverter, a source coupled to a ground node, and a gate that receives the sense amplifier enable signal.

6. A device according to Claim 5, wherein the first transistor comprises an NMOS transistor having a source coupled to the data line, and wherein the second transistor comprises a PMOS transistor having a drain coupled to a drain of the NMOS transistor and a source coupled to the power supply node.

7. A device according to Claim 1:

wherein the data line is coupled to an input of the buffer;

wherein the output buffer comprises an inverter operative to be enabled and disabled responsive to the sense amplifier enable signal; and

wherein the sense amplifier circuit comprises a transistor coupled between the data line and the power supply node and having a gate that receives the sense amplifier enable signal.

8. A device according to Claim 1, wherein the cell select circuitry is configured to selectively couple the memory cells to a plurality of bit lines responsive to signals on word lines, and wherein the cell select circuitry includes a gate circuit that selectively couples the bit lines to the data line responsive to a plurality of column select signals.

9. A memory device comprising:

a memory cell array with a plurality of memory cells connected to a plurality of word lines and operative to be selectively connnected to a plurality of bit lines responsive to signals on the word lines;

a pre-discharge circuit that predischarges the plurality of bit lines during a pre-discharge operation;

a data input and output gate circuit that transmits data between the plurality of bit lines and a plurality of data lines during a read operation; and

a sense amplifier including a bias circuit that biases the data lines to a bias voltage level in response to a bias control signal during the read operation, and an amplifier circuit that detects and amplifies voltage changes on the plurality of data lines and that responsively generates a sense output signal subject to a sense amplifier enable signal during the read operation.

10. A device according to Claim 9, wherein the bias circuit comprises:

a first transistor connected between a power supply voltage and the data line;

a second transistor being turned on in response to the bias control signal for turning off the first transistor during the pre-discharge operation, and being turned on when the sense amplifier enable signal is enabled during the read operation; and

a first buffer being enabled in response to the bias control signal for buffering a voltage signal of the data line during the read operation, and being disabled when the sense amplifier enable signal is enabled during the read operation.

11. A device according to Claim 10, wherein the first and second transistors comprise respective PMOS transistors.

12. A device according to Claim 10, wherein the first buffer generates a signal with a power supply voltage when a voltage of the data line is greater than the bias voltage, and generates the signal with a ground voltage when the voltage of the data line is lower than the bias voltage.

13. A device according to Claim 9, wherein the sense amplifier circuit comprises:

a third transistor that is connected between a power supply voltage and a first node and that supplies a current to the first node;

an inverter operative to be enabled in response to the sense amplifier enable signal and that inverts a voltage level of the data line and transmits the inverted voltage level to a second node;

a fourth transistor connected between the second node and a ground voltage and operative to be turned off in response to the sense amplifier enable signal during the read operation;

a fifth transistor connected between the first node and the data line and operative to be turned on in response to a voltage signal of the second node to let a current flow from the first node to the data line; and

a second buffer operative to be enabled in response to the sense amplifier enable signal and to buffer a signal of the first node and responsively generate the sense output signal.

14. A device according to Claim 13, wherein a transconductance of the fifth transistor is greater than a transconductance of the third transistor.

15. A device according to Claim 13, wherein the third transistor is a PMOS transistor.

16. A device according to Claim 13, wherein the fifth and fourth transistors comprise respective NMOS transistors.

17. A device according to Claim 13, wherein the inverter generates a signal with a ground voltage when a voltage of the data line is greater than the bias voltage, and generates the signal with a power supply voltage when a voltage of the data line is lower than the bias voltage.

18. A device according to Claim 9, wherein the sense amplifier circuit comprises:

a third transistor that is connected between a power supply voltage and a first node and that supplies a current to the first node;

a fourth transistor that is connected between the first node and the data line and that supplies a current to the data line by being turned on in response to the sense amplifier enable signal; and

a second buffer operative to be enabled in response to the sense amplifier enable signal and to buffer a voltage signal of the data line to generate the sense output signal.

19. A device according to Claim 18, wherein the third and fourth transistors comprise respective PMOS transistors.

20. A device according to Claim 18, wherein the second buffer generates the sense output signal with a ground voltage when a voltage level of the data line is lower than that of the bias voltage, and generates the sense output signal with a power supply voltage when a voltage level of the data line is higher than that of the bias voltage.

21. A sense amplifier comprising:

a bias circuit that biases a sense input signal terminal to a bias voltage level in response to a bias control signal; and

a sense amplifier circuit that generates a sense output signal by detecting and amplifying a change of the bias voltage level of the sense input signal terminal in response to a sense amplifier enable signal.

22. A sense amplifier according to Claim 21, wherein the bias circuit comprises:

a first transistor connected between a power supply voltage and the sense input signal terminal;

a second transistor that turns off the first transistor by being turned on in response to the bias control signal and by being turned on when the sense amplifier enable signal is enabled; and

a first buffer operative to be enabled in response to the bias control signal and to buffer a voltage of the sense input signal terminal, and to be disabled when the sense amplifier enable signal is enabled.

23. A sense amplifier according to Claim 22, wherein the first and second transistors comprise respective PMOS transistors.

24. A sense amplifier according to Claim 22, wherein the first buffer generates a signal with a power supply voltage if a voltage of the sense input signal

terminal is greater than the bias voltage and generates the signal with a ground voltage if a voltage of the sense input signal terminal is less than the bias voltage.

25. A sense amplifier according to Claim 21, wherein the sense amplifier circuit comprises:

a third transistor that is connected between a power supply voltage and a first node and that supplies a current to the first node;

an inverter operative to be enabled in response to the sense amplifier enable signal and to invert a voltage level of the data line and to transmit the inverted voltage level to a second node;

a fourth transistor connected between the second node and a ground voltage and operative to be turned off in response to the sense amplifier enable signal;

a fifth transistor connected between the first node and the sense input signal terminal and operative to be turned on in response to a signal of the second node to let a current flow from the first node to the sense input signal terminal; and

a second buffer operative to be enabled in response to the sense amplifier enable signal and to buffer a signal of the first node to generate the sense output signal.

26. A sense amplifier according to Claim 25, wherein a transconductance of the fifth transistor is greater than a transconductance of the third transistor.

27. A sense amplifier according to Claim 26, wherein the third transistor is a PMOS transistor.

28. A sense amplifier according to Claim 25, wherein the fifth and fourth transistors comprise respective NMOS transistors.

29. A sense amplifier according to Claim 25, wherein the inverter generates a signal with a ground voltage when a voltage of the sense input signal terminal is greater than the bias voltage, and generates the signal with a power supply voltage when a voltage of the sense input signal terminal is lower than the bias voltage.

30. A sense amplifier according to Claim 21, wherein the sense amplifier circuit comprises:

a third transistor that is connected between a power supply voltage and a first node and that supplies a current to the first node;

a fourth transistor that is connected between the first node and the sense input signal terminal and that supplies a current to the sense input signal terminal line by being turned on in response to the sense amplifier enable signal; and

a second buffer operative to be enabled in response to the sense amplifier enable signal and to buffer a voltage signal of the sense input signal terminal to generate the sense output signal.

31. A sense amplifier according to Claim 30, wherein the third and fourth transistors comprise respective PMOS transistors.

32. A sense amplifier according to Claim 30, wherein the second buffer generates the sense output signal with a ground voltage when a voltage level of the sense input signal terminal is lower than that of the bias voltage, and generates the sense output signal with a power supply voltage when a voltage level of the sense input signal terminal is higher than that of the bias voltage.